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EXAMINER
CHU, GABRIEL L

ART UNIT	PAPER NUMBER
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,333	STATON ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34 and 40-47* is/are rejected.

7)☒ Claim(s) *35-39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20041122*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claims 33 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim.**

Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The apparatus of claim 14 comprises the software programming interface and claim 14 already stores.

2. **Claims 5-9, 14-20, 22, 25, 27-31, 34, 45 objected to because of the following informalities:**

Referring to claim 5, 6, "the software programming interface" is understood to refer to "the programming interface".

Referring to claim 7, "component to create" is understood to refer to "component creates".

Referring to claim 8, "the particular" is understood to refer to "a particular".

Referring to claim 9, "the particular data" is understood to refer to "the particular data type".

Referring to claim 14-19, 22, 25, 28, every instance (in some claims there are more than one) of "the monitor components" is understood to refer to "the one or more interconnect monitor components".

Referring to claim 15, "calls" is understood to refer to "call", "the code" is understood to refer to "code", "the simulation run" is understood to refer to "a simulation run", "a simulation run" is understood to refer to "the simulation run".

Referring to claim 16, "the code" is understood to refer to "code"

Referring to claim 17, "supplies" is understood to refer to "supply", "the two or more checker components" is understood to refer to "the two or more checker components to verify an interconnect protocol".

Referring to claim 20, "the programming interface" is understood to refer to "the software programming interface".

Referring to claim 22, "supplies" is understood to refer to "supply",

Referring to claim 27, "the software monitor component" is understood to refer to "the one or more interconnect monitor components".

Referring to claim 29, "the programming interface component" is understood to refer to "the software programming interface".

Referring to claim 30, "the functional checker component" is understood to refer to "the one or more functional checker components".

Referring to claim 31, "all of the hardware" is understood to refer to "all hardware", "that connection" is understood to refer to "that interconnection".

Referring to claim 34, "A method, comprising" is understood to refer to "A method comprising", "the code" is understood to refer to "code".

Referring to claim 45, "the monitor component" is understood to refer to "the interconnect monitor component".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claim 1-11, 13, 15 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.** Referring to claims 1-11, 13, it is unclear how a computer readable medium with code stored on it in combination with disembodied software constitutes an "apparatus" in even its broadest reasonable sense.

5. Referring to claim 15, it is not clear to which checker component "the checker component" refers.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. **Claims 1-33, 40-47 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.**

8. Referring to claims 1-13, Applicant has claimed, in part, a computer readable medium storing code for a functional checker and, in part, a protocol checker, monitor, and interface. These mediums are understood to refer to page 23 of the specification wherein what is considered to be such a medium is defined. Since neither the components nor the interface are claimed in combination with the necessary hardware to enable their functionality, the claim is to an abstract idea rather than a practical

application of the idea, since no physical transformation nor useful, concrete and tangible result would be able to be realized from the idea of what is claimed.

Further, in claim 12, Applicant has claimed that the apparatus of claim 1 is stored on a "machine-readable" medium. Even if the limitations or claim 1 are now all embodied on such a medium, Applicant has specifically disclosed that such a medium may not be limited to storage mediums, but also include transmission mediums. Applicant must amend the claims to include only storage mediums, and amend the specification to distinguish between machine/computer readable mediums as storage and transmission mediums. It is further evident from this same paragraph that Applicant considers such transmission mediums as storage ("...or any type of media suitable for storing"), thereby negating "storing" as limiting to storage media.

9. Referring to claims 14-33, 45-47, Applicant has specifically disclosed that a machine-readable medium may not be limited to storage mediums, but also include transmission mediums. Applicant must amend the claims to include only storage mediums, and amend the specification to distinguish between machine/computer readable mediums as storage and transmission mediums. It is further evident from this same paragraph that Applicant considers such transmission mediums as storage ("...or any type of media suitable for storing"), thereby negating "storing" as limiting to storage media.

10. Referring to claim 40-44, such "means" are understood to refer to disembodied software means as evidenced by page 23. In order to overcome this rejection, these claims must be amended to limit to software embodied on a storage medium.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. **Claims 34 and 40 rejected under 35 U.S.C. 103(a) as being unpatentable over US 6678645 to Rajsuman et al in view of US 6292765 to Ho et al. and "object-oriented" by Microsoft Computer Dictionary (MSCD).** Referring to claim 34, 40, Rajsuman discloses monitoring a hardware interconnect between two or more IP cores to collect protocol data (From line 52 of column 10, "In the proposed method, verification of this logic is done by the dedicated sub-system as indicated in FIG. 5 by the design validation station DVS.sub.6 for verification of glue logic. The basic methodology is as follows: (1) Use interconnect bus 71 that connects various silicon ICs 68 as shown in FIG. 5 to model the SoC on-chip bus. This is a system bus that connects various cores A-E which models the behavior of the on-chip bus. This maps instruction and data flow at an SoC level (from one core to another core) onto instruction and data flow at a design validation station level (from one VU to another VU). Hence, this bus captures any request/grant protocol of the SoC on-chip bus as well as all data transactions at each interface of the individual cores.");

generating a data structure to pass protocol data to two or more locations associated with checker components (From line 62 of column 10, "Hence, this bus captures any request/grant protocol of the SoC on-chip bus as well as all data

transactions at each interface of the individual cores." Wherein request/grant protocol and data transactions are captured, wherein such data occupy "locations". From line 4 of column 11, "FIG. 7 shows the emulator sub-system. In this approach, any commercial emulator system can be used. In FIG. 7, the emulator 72 is loaded with the synthesizable RTL of glue logic and with the testbench data in the glue logic testbench file 77. The synchronization unit and arbitration units are used with commercial emulator to interface it with other VUs 66.");

and calling methods defined in code of the checker components for data for a simulation run (From line 52 of column 10, "In the proposed method, verification of this logic is done by the dedicated sub-system as indicated in FIG. 5 by the design validation station DVS.sub.6 for verification of glue logic." Further, from line 8 of column 11, "The synchronization unit and arbitration units are used with commercial emulator to interface it with other VUs 66.")

Although Rajsuman does not specifically disclose that such a data structure may be object oriented, OO data structures are well known in the art. An example of this is shown by MSCD, "Of, pertaining to, or being a system or language that supports the use of objects." A person of ordinary skill in the art at the time of the invention would have been motivated to use an OO data structure because data is an object, and also because, from figure 7, C++, an OO language, is disclosed as a language used in the system.

Although Rajsuman does not specifically disclose checking as data becomes available during a simulation run, testing during simulation is known in the art. An

example of this is shown by Ho, from line 61 of column 4, "In one embodiment, the programmed computer automatically generates descriptions of additional circuits (hereinafter "checkers") that monitor portions of the circuit-under-verification, and flag behaviors of the portions in conformance with known defective behaviors. During simulation, each checker is coupled to an instance of an arrangement of circuit elements associated with a defective behavior. Each checker monitors signals flowing to and from the instance and generates an error message on detecting the known defective behavior. Use of automatically generated checkers in combination with automatic state restoration and simulation as described herein has several advantages. Specifically, the checkers flag an error as soon as the error occurs in simulation, emulation, or in a semiconductor die, because each checker monitors defective behavior of one instance of an arrangement in the circuit. Therefore, diagnosing errors flagged by automatically generated checkers is much easier than diagnosing errors flagged by end-to-end tests. Furthermore, functional verification can be terminated as soon as an error message is generated, thereby eliminating the generation and diagnosis of additional error messages (generated by continuing the functional verification). Hence, use of checkers as described herein eliminates the prior art need to simulate after an error occurs (e.g. in some cases for several hours) until an effect of the error is detected by an end-to-end test." A person of ordinary skill in the art at the time of the invention would have been motivated to test during simulation because, as disclosed above by Ho, "diagnosing errors flagged by automatically generated checkers is much easier than diagnosing errors flagged by end-to-end tests" and "functional

verification can be terminated as soon as an error message is generated, thereby eliminating the generation and diagnosis of additional error messages (generated by continuing the functional verification)".

Allowable Subject Matter

13. **Claims 35-39 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.** Referring to claim 35, the prior art does not teach or fairly suggest, receiving a type of data requested and a location to send that data from the checker at the start of the simulation run.

14. Referring to claim 36, the prior art does not teach or fairly suggest, providing callback services to the checker component at registration.

15. Referring to claim 37, the prior art does not teach or fairly suggest, generating a data item that is self maintaining and will delete itself once all checker components are no longer referencing that data item.

16. Referring to claim 38, the prior art does not teach or fairly suggest, using data structures that use shared pointers to pass data to locations in two or more checker components.

17. Referring to claim 39, the prior art does not teach or fairly suggest, using data structures that use shared pointers to pass data to two or more locations within a checker component.

18. **Claims 1-32, 45-47 rejected/objected as detailed above, but would be allowable if rewritten to overcome the rejections/objections.** Referring to claims 1-13, 45-47, the prior art does not teach or fairly suggest the interconnect monitor component having code to build data structures containing protocol data types requested by a first checker component and code specifying where to deliver data based upon a particular type of data requested by the first checker component, in the scope and context of claim 1, 45.

19. Referring to claims 14-32, the prior art does not teach or fairly suggest the monitor components have code to create protocol data objects that track within themselves whether their data is still being used by another checker component and when their protocol data object should be deleted, in the scope and context of claim 1.

20. **Claims 41-44 rejected and objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and further rewritten to overcome the rejections.** Referring to claim 41, the prior art does not teach or fairly suggest means for receiving a type of data requested and a location to send that data from the checker anytime during the simulation run.

21. Referring to claim 42, the prior art does not teach or fairly suggest means for providing callback services to the checker component at registration.

22. Referring to claim 43, the prior art does not teach or fairly suggest means for generating a data item that is self maintaining and will delete itself once all checker components are no longer referencing that data item.

23. Referring to claim 44, the prior art does not teach or fairly suggest means for using data structures that use shared pointers to pass data to locations in two or more checker components.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See notice of references cited.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gabriel L. Chu
Examiner
Art Unit 2114

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